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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/750,157	12/30/2003	Carlos J. Gonzalez	SNDK.348US0	7914
66785	7590	09/15/2010		
DAVIS WRIGHT TREMAINE LLP - SANDISK CORPORATION			EXAMINER	
505 MONTGOMERY STREET			LI, ZHUO H	
SUITE 800				
SAN FRANCISCO, CA 94111			ART UNIT	PAPER NUMBER
			2185	
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			09/15/2010	PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b> 10/750,157	<b>Applicant(s)</b> GONZALEZ ET AL.	
	<b>Examiner</b> ZHUO H. LI	<b>Art Unit</b> 2185	

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 06 July 2010.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 44-51 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 44-51 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftperson's Patent Drawing Review (PTO-948)   | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date <u>7/6/10</u> . | 6) <input type="checkbox"/> Other: _____  |

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## **DETAILED ACTION**

### ***Response to Amendment***

1. This Office action is in response to the amendment filed on July 6, 2010, claims 44-51 are pending in the application.

### ***Information Disclosure Statement***

2. The Information Disclosure Statement filed on July 6, 2010 has been considered.

### ***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later

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invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 44-51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Conley (US 2002/0099904) in view of Chien et al. (US 6,742,078 hereinafter Chien) and Kakinuma et al. (US 6,581,132 hereinafter Kakinuma).

Regarding claim 44, Conley discloses a method of operating a memory system as shown in figure 2 including a controller (301, figure 2) and a non-volatile memory, i.e., flash memory (figure 2), the non-volatile memory having a plurality of units of erases (85-88, figure 15), the method comprising establishing by a controller (450, figure 1) of an initial set of metablock linkings by which the controller accesses the non-volatile memory ([0038]-[0039]), each metablock linking comprised of a composite logical linking of a plurality of units of erase and where the controller forms said initial set of metablock linkings according to a rule ([0066], the controller programming of data into at least one page of each of the blocks forming the metablock) and subsequently updating the record of the first linking in the non-volatile memory to reflect the updating of the first metablock linking ([0067], use additional blocks to update a data file stored in the metablock, where the update reflect the linking between metablock). Conley differs from the claimed invention in not specifically teaching the steps of subsequently determining that one or more units of erase in a first metablock linking of the initial set of metablock linkings is defective and updating the first metablock linking so that it no longer contains said defective one of more units of erase. However, Chien discloses a flash memory

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system comprising four different types of blocks, data blocks, spare blocks, a new block and a link-table blocks (col. 2 lines 35-53), wherein the link-table blocks comprising a link table which it is used to record the link relationship between the logic block and the actual block (col. 3 lines 51-57 and col. 4 line 55 through col. 5 line 3). In addition, Chien further discloses the method comprising subsequently determining that one or more units of erase in a first metablock linking of initial set of metablock linkings is defective (col. 3 lines 43-46), and updating the first metablock linking so that it no longer contains the defective one or more units of erase, i.e., stored updated data in a substituted block (col. 3 line 63 through col. 4 line 20). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Conley in having the steps of subsequently determining that one or more units of erase in a first metablock linking of the initial set of metablock linkings is defective and updating the first metablock linking so that it no longer contains said defective one or more units of erase, as per teaching of Chien, because it provides protection against power failure to protect the data link structure and improves stability (see Chien, col. 1 lines 12-15). Furthermore, the combination of Conley and Chien differs from the claimed invention in not specifically teaching the controller access data identified by currently active logical address on the non-volatile memory, maintaining a record of the metablock linkings in non-volatile memory, wherein the record only includes deviations from the rule so that updating the first metablock linking deviates from the rule and no longer contains the defective one or more units of erase. However, Kakinuma teaches to a memory system comprising a controller (34, figure 13) accesses data identified by currently active logic address on a non-volatile memory (col. 15 lines 18-24 and lines 57-67), maintaining a record of the metablock linkings in non-volatile memory (col. 5 lines

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51-59, maintaining a conversion table in a storage medium), wherein the record only includes deviations from the rule (col. 7 lines 19-31, correspondence of both logical block address and physical block address) so that updating the first metablock linking deviates from the rule and no longer contains the defective one or more units of erase (col. 5 lines 39-50 and col. 7 lines 32-55) in order to adequately manage defective sectors for operating the memory system at a high speed (col. 2 lines 15-19). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the combination of Conley and Chien in having the controller access data identified by currently active logical address on the non-volatile memory, maintaining a record of the metablock linkings in non-volatile memory, wherein the record only includes deviations from the rule so that updating the first metablock linking deviates from the rule and no longer contains the defective one or more units of erase, as per teaching of Kakinuma, in order to adequately manage defective sectors for operating the memory system at a high speed.

Regarding claim 45, Chien teaches updating the first metablock linking including replacing the one or more defective units of erase with non-defective units of erase (col. 3 line 43 through col. 4 line 20).

Regarding claim 46, Chien teaches said non-defective units of erase being selected from a list of unlinked units of erase (col. 3 line 63 through col. 4 line 3).

Regarding claim 47, Chien teaches said list of unlinked units of erase being maintained in the non-volatile memory (figure 1 and col. 3 lines 8-30).

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Regarding claim 48, Chien discloses subsequent to said replacing the defective unit of erase with non-defective units of erase (col. 3 lines 22-41), updating said list of unlinked units of erase (col. 5 lines 18-45).

Regarding claim 49, Chien discloses said non-defective units of erase being selected from a unit of erase formerly belonging to another linking (col. 4 lines 4-20).

Regarding claim 50, Conley teaches said rule being implemented by firmware on the memory system ([0038]).

Regarding claim 51, Chien further discloses the method further comprising determining that one or more units of erase in a first metablock linking of initial set of metablock linkings is defective (col. 3 lines 43-46), and further updating the first metablock linking so that it no longer contains the defective one or more units of erase, i.e., stored updated data in a substituted block (col. 3 line 63 through col. 4 line 20); and Conley teaches subsequently updating the record of the first linking in the non-volatile memory to reflect the updating of the first metablock linking ([0067], use additional blocks to update a data file stored in the metablock, where the update reflect the linking between metablock). Thus, the claimed limitations are rejected under the combination of Coley, Chien and Kakinuma.

### ***Response to Arguments***

5. Applicant's arguments with respect to claims 44-51 have been considered but are moot in view of the new ground(s) of rejection.

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***Conclusion***

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to ZHUO H. LI whose telephone number is (571)272-4183. The examiner can normally be reached on Mon and Tue 6:00am - 2:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on 571-272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Zhuo H Li/

Examiner, Art Unit 2185

/Tuan V. Thai/

Primary Examiner, Art Unit 2185